What Is Claimed Is:

1. An apparatus for detecting errors on a source-synchronous bus, comprising:

the source-synchronous bus, wherein the source-synchronous bus includes a plurality of data lines and a clock line;

a transmitting mechanism coupled to the source-synchronous bus, wherein the transmitting mechanism is configured to transmit data on the source-synchronous bus;

a receiving mechanism coupled to the source-synchronous bus, wherein the receiving mechanism is configured to receive data from the source-synchronous bus; and

an error detecting mechanism coupled to the receiving mechanism that is configured to detect errors on the source-synchronous bus;

wherein the error detecting mechanism can detect errors on the plurality of data lines including errors that are caused by an error on the clock line.

2. The apparatus of claim 1, wherein the apparatus further comprises:

a grouping mechanism coupled to the transmitting mechanism that is configured to group data bits into an error group;

a detection code generating mechanism coupled to the grouping mechanism that is configured to generate a detection code for the error group; and

the transmitting mechanism that is further configured to transmit the detection code on the source-synchronous bus using a clock cycle other than the clock cycles used for transmitting data bits of the error group.

3. The apparatus of claim 2, wherein the detection code is a parity bit.

4. The apparatus of claim 2, wherein the detection code is an error correcting code.

5. The apparatus of claim 2, wherein the grouping mechanism is further configured to skew data bits within the error group across time.

6. The apparatus of claim 5, wherein skewing data bits across time includes delaying a data bit based on a position of the data bit within the error group.

7. The apparatus of claim 5, further comprising a gathering mechanism coupled to the receiving mechanism, wherein the gathering mechanism is configured to de-skew data bits within the error group.

8. A method for detecting errors on a source-synchronous bus, wherein the source-synchronous bus includes a plurality of data lines and a clock line, the method comprising:

transmitting data from a source on the source-synchronous bus;

receiving data at a destination from the source-synchronous bus; and

detecting data errors at the destination, wherein detecting data errors includes detecting errors that are caused by errors on the clock line.

9. The method of claim 8, further comprising:

grouping data bits into an error group;

generating a detection code for the error group; and

transmitting the detection code on the source-synchronous bus using a clock cycle other than the clock cycles used for transmitting data bits of the error group.

10. The method of claim 9, wherein the detection code is a parity bit.

11. The method of claim 9, wherein the detection code is an error correcting code.

12. The method of claim 9, further comprising skewing data bits within the error group across time.

13. The method of claim 12, wherein skewing data bits across time includes delaying a data bit based on a position of the data bit within the error group.

14. The method of claim 12, further comprising de-skewing data bits within the error group.

15. A computing system for detecting errors on a source-synchronous bus, comprising:

the source-synchronous bus, wherein the source-synchronous bus includes a plurality of data lines and a clock line;

a central processing unit coupled to the source-synchronous bus, wherein the central processing unit is configured to transmit data on the source-synchronous bus;

a memory unit coupled to the source-synchronous bus, wherein the memory unit is configured to receive data from the source-synchronous bus; and

an error detecting mechanism coupled to the memory unit that is configured to detect errors on the source-synchronous bus;

wherein the error detecting mechanism can detect errors on the plurality of data lines including errors that are caused by an error on the clock line.

16. The computing system of claim 15, wherein the computing system further comprises:

a grouping mechanism coupled to the central processing unit that is configured to group data bits into an error group;

a detection code generating mechanism coupled to the grouping mechanism that is configured to generate a detection code for the error group; and

the central processing unit that is further configured to transmit the detection code on the source-synchronous bus using a clock cycle other than the clock cycle used for the error group.

17. The computing system of claim 16, wherein the detection code is a parity bit.

18. The computing system of claim 16, wherein the detection code is an error correcting code.

19. The computing system of claim 16, wherein the grouping mechanism is further configured to skew data bits within the error group across time.

20. The computing system of claim 19, wherein skewing data bits across time includes delaying a data bit based on a position of the data bit within the error group.

21. The computing system of claim 19, further comprising a gathering mechanism coupled to the memory unit, wherein the gathering mechanism is configured to de-skew data bits within the error group.